45 HOURS LECTURE SCHEDULE

Unit No.	Lecture schedule	Hours
Unit 1	Introduction to ARM architecture family, Condition Flags, Reset, Register set	**3**
	ARM Core Dataflow model, ARM 3 stage and 5-stage pipeline organization	**2**
Unit 2	ARM Instruction Set	**11**
	ARM Assembly Language Programming Examples	**1.5**
	Thumb Instructions, ARM interrupt Processing and handling schemes	**5.5**
Unit 3	ARM coprocessor interface and Instructions, Floating Point Format and VFP	**6**
Unit 4	Memory hierarchy- Cache Memory Organization in ARM	**5**
	Memory Protection Units (MPU), Virtual Memory, Memory Mgt (MMU) in ARM	**4**
Unit 5	Architectural support for System Development, ARM programming tools	**3**
	AMBA architecture (ASB, AHB, APB)	**1**
	Peripherals (DMA, RTC, ADC, DAC and PWM)	**1**
	I2C and SPI protocols , USART and GPIO	**1**
	Other ARM Processor cores (ARM9, ARM10, ARM11) and Advanced Features	**1**
	Total	**45**

45 HOURS LECTURE PLAN:

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45 Hours Lecture Plan			
Session	**Topics Covered**	**Hours**	**Learning Outcome**
1	Types of computer Architectures, ISA's and ARM History	1	L1,L2
2	Embedded System Software and Hardware, stack implementation in ARM, Endianness, condition codes	1	L3,L4
3	Processor core VS CPU core, ARM7TDMI Interface signals, Memory Interface, Bus Cycle types, Register set, Operational Modes	1	L1,L3,L4,L6
4	Instruction Format, ARM Core Data Flow Model, ARM 3 stage Pipeline, ARM family attribute comparision	1	L3,L4,L6
5	ARM 5 stage Pipeline, Pipeline Hazards, Data forwarding - a hardware solution	1	L3,L4,L6
6	ARM ISA and Processor Variants, Different Types of Instructions, ARM Instruction set, data processing instructions	1	L3,L4,L6
7	Shift Operations, shift Operations using RS lower byte, Immediate value encoding	1.5	L1,L2,L3
8	Dataprocessing Instructions	1	L1,L2,L3
9	AddressingMode-1, Addressing Mode -2	1	L1,L2,L3
10	Addressing Mode -2, LDR/STR, Addressing mode -3 with examples	1.5	L1,L2,L3
11	Instruction Timing, Addressing Mode - 4 with Examples	1.5	L1,L2,L3
12	Swap Instructions, Swap Register related Instructions, Loading Constants	1	L1,L2,L3
13	Program Control Flow, Control Flow Instructions, B & BL instructions, BX instruction	1	L1,L2,L3
14	Interrupts and Exceptions, Exception Handlers, Reset Handling	1.5	L1,L2,L3
15	Aborts, software Interrupt Instruction, undefined instruction exception	1.5	L1,L2,L3
16	Interrupt Latency, Multiply Instructions, Instruction set examples	1	L1,L2,L3,L5
17	Thumb state, Thumb Programmers model, Thumb Implementation, Thumb Applications	1	L1,L2,L3,L5
18	Thumb Instructions, Interrupt processing	1.5	L1,L2,L3,L5
19	Interrupt Handelling schemes, Examples of Interrupt Handlers	2	L1,L2,L3,L5
20	Coprocessors	1.5	L3,L5,L6
21	Coprocessor Instructions, data Processign Instruction, data transfers, register transfers	1.5	L3,L5,L6
22	Number representations, floating point representation	1.5	L3,L5
23	Flynn's Taxonomy, SIMD and Vector Processors, Vector Floating Point Processor (VFP), VFP and ARM interactions, An example vector operation	1.5	L3,L5
24	Memory Technologies, Need for memory Hierarchy, Hierarchical Memory Organization, Virtual Memory	1.5	L3,L4
25	Cache Memory, Mapping Functions	2	L3,L4
26	Cache Design, Unified or split cache, multiple level of caches, ARM cache features, coprocessor 15 for system control	1.5	L3,L4

27	Processes, Memory Map, Protected Systems, ARM systems with MPU, memory Protection Unit (MPU)	1.5	L3,L4
28	Physical Vs Virtual Memory, Paging, Segmentation	1	L3,L4
29	MMU Advantage, virtual memory translation, Multitasking with MMU, MMU organization, Tightly coupled Memory (TCM)	1.5	L3,L4,L5,L6
30	ARM Development Environment, Arm Procedure Call Standard (APCS), Example C program	2	L3,L5,L6
31	Embedded software Development, Image structure, linker inputs and outputs, memory map, application startup	1	L3,L5,L6
32	AMBA Overview, Typical AMAB Based Microcontroller, AHB bus features, AHB Bus transfers, APB bus transfers, APB bridge	1	L3,L5,L6
33	DMA, Peripherals, Programming Peripherals in ARM	1	L3,L5,L6
34	Protocols (I2c, SPI), UART, GPIO	1	L3,L5,L6
35	ARM ISAs, ARMv5, ARMv6, ARM v7, big.little technology, ARMv8	1	L3,L5,L6
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